CLA 16-BIT Circuit 7nm finfet technology

.option post

.option measdgt=6

.temp 27

.param pulsew=10n delay=10p loadc=1f LenTran='7\*pulsew' vdd=1.0v

.param tbsi=8.6n

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*TRANSITIONS\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.tran 10p LenTran

\*.tran 10p LenTran sweep vdd 0.85v 1.1v 0.05v

\*.tran 10p LenTran sweep wmin 0.13u 2u 0.02u

\*.tran 10p LenTran sweep k1 1 4 0.1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* TRANSISTOR SIZING \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.param lmin=7n

\*.param k1=2

\*.param wp1='wmin\*k1' wn1='wmin\*k2'

\*.param a0=0 a1=vdd a2=0 a3=vdd

\*.param b0=vdd b1=vdd b2=vdd b3=vdd

\*.param c0=0

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

vdd vdd 0 vdd

.global vdd 0

.include '/home /pradeep/7nm\_pmos.lib'

.include '/home /pradeep/7nm\_nmos.lib'

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* CIRCUIT DESIGN \*\*\*\*\*\*\*\*\*\*\*

va a0 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '6\*pulsew' 0)

vb b0 0 pwl (0p vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vc a1 0 pwl (0p 0v, '1\*pulsew' 0v, '1\*pulsew+delay' vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vd b1 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

ve a2 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vf b2 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vg a3 0 pwl (0p 0v, '1\*pulsew' 0v, '1\*pulsew+delay' vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vh b3 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '6\*pulsew' 0v)

vi a4 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '6\*pulsew' 0)

vj b4 0 pwl (0p vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vk a5 0 pwl (0p 0v, '1\*pulsew' 0v, '1\*pulsew+delay' vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vl b5 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vm a6 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vn b6 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vo a7 0 pwl (0p 0v, '1\*pulsew' 0v, '1\*pulsew+delay' vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vp b7 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '6\*pulsew' 0v)

vq a8 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '6\*pulsew' 0)

vr b8 0 pwl (0p vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vs a9 0 pwl (0p 0v, '1\*pulsew' 0v, '1\*pulsew+delay' vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vt b9 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vu a10 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vv b10 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vw a11 0 pwl (0p 0v, '1\*pulsew' 0v, '1\*pulsew+delay' vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vx b11 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '6\*pulsew' 0v)

vy a12 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '6\*pulsew' 0)

vz b12 0 pwl (0p vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vaa a13 0 pwl (0p 0v, '1\*pulsew' 0v, '1\*pulsew+delay' vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vab b13 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vac a14 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vad b14 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd, '6\*pulsew+delay' 0v)

vae a15 0 pwl (0p 0v, '1\*pulsew' 0v, '1\*pulsew+delay' vdd, '3\*pulsew' vdd, '3\*pulsew+delay' 0v, '5\*pulsew' 0v, '5\*pulsew+delay' vdd, '6\*pulsew' vdd)

vaf b15 0 pwl (0p vdd, '4\*pulsew' vdd, '4\*pulsew+delay' 0v, '6\*pulsew' 0v)

vag c0 0 pwl (0p 0v, '6\*pulsew' 0v)

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* MOS TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.subckt XOR A B OUT

mp1 N6 A vdd vdd pfet w=10n l=lmin

mn2 N6 A 0 0 nfet w=10n l=lmin

mn9 OUT A N10 0 nfet w=10n l=lmin

mn11 N10 B 0 0 nfet w=10n l=lmin

mn10 OUT N6 N2 0 nfet w=10n l=lmin

mn12 N2 N4 0 0 nfet w=10n l=lmin

mn4 N4 B 0 0 nfet w=10n l=lmin

mp7 OUT N6 N9 vdd pfet w=10n l=lmin

mp8 OUT N4 N9 vdd pfet w=10n l=lmin

mp5 N9 A vdd vdd pfet w=10n l=lmin

mp6 N9 B vdd vdd pfet w=10n l=lmin

mp3 N4 B vdd vdd pfet w=10n l=lmin

.ends

.subckt AND2in A B OUT

mp1 OUT1 A vdd vdd pfet w=10n l=lmin

mp2 OUT1 B vdd vdd pfet w=10n l=lmin

mp3 OUT OUT1 vdd vdd pfet w=10n l=lmin

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* nfet TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mn1 OUT1 A A AA 0 nfet w=10n l=lmin

mn2 AA B 0 0 nfet w=10n l=lmin

mn3 OUT OUT1 0 0 nfet w=10n l=lmin

.ends

.subckt AND3in A B C OUT

mp1 OUT1 A vdd vdd pfet w=10n l=lmin

mp2 OUT1 B vdd vdd pfet w=10n l=lmin

mp3 OUT1 C vdd vdd pfet w=10n l=lmin

mp4 OUT OUT1 vdd vdd pfet w=10n l=lmin

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* nfet TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mn1 OUT1 A AA 0 nfet w=10n l=lmin

mn2 AA B BB 0 nfet w=10n l=lmin

mn3 BB C 0 0 nfet w=10n l=lmin

mn4 OUT OUT1 0 0 nfet w=10n l=lmin

.ends

.subckt AND4in A B C D OUT

mp1 OUT1 A vdd vdd pfet w=10n l=lmin

mp2 OUT1 B vdd vdd pfet w=10n l=lmin

mp3 OUT1 C vdd vdd pfet w=10n l=lmin

mp4 OUT1 D vdd vdd pfet w=10n l=lmin

mp5 OUT OUT1 vdd vdd pfet w=10n l=lmin

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* nfet TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mn1 OUT1 A AA 0 nfet w=10n l=lmin

mn2 AA B BB 0 nfet w=10n l=lmin

mn3 BB C CC 0 nfet w=10n l=lmin

mn4 CC D 0 0 nfet w=10n l=lmin

mn5 OUT OUT1 0 0 nfet w=10n l=lmin

.ends

\*.subckt AND5in A B C D E OUT

\*mp1 OUT1 A vdd vdd pfet w=10n l=lmin

\*mp2 OUT1 B vdd vdd pfet w=10n l=lmin

\*mp3 OUT1 C vdd vdd pfet w=10n l=lmin

\*mp4 OUT1 D vdd vdd pfet w=10n l=lmin

\*mp5 OUT1 E vdd vdd pfet w=10n l=lmin

\*mp6 OUT OUT1 vdd vdd pfet w=10n l=lmin

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* nfet TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*mn1 OUT1 A AA 0 nfet w=10n l=lmin

\*mn2 AA B BB 0 nfet w=10n l=lmin

\*mn3 BB C CC 0 nfet w=10n l=lmin

\*mn4 CC D DD 0 nfet w=10n l=lmin

\*mn5 DD E 0 0 nfet w=10n l=lmin

\*mn6 OUT OUT1 0 0 nfet w=10n l=lmin

\*.ends

.subckt OR2in A B OUT

mp1 AA A vdd vdd pfet w=10n l=lmin

mp2 OUTN B AA vdd pfet w=10n l=lmin

mp3 OUT OUTN vdd vdd pfet w=10n l=lmin

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* nfet TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mn1 OUTN A 0 0 nfet w=10n l=lmin

mn2 OUTN B 0 0 nfet w=10n l=lmin

mn3 OUT OUTN 0 0 nfet w=10n l=lmin

.ends

.subckt OR3in A B C OUT

mp1 OUTN A vdd 0 nfet w=10n l=lmin

mp2 OUTN B vdd 0 nfet w=10n l=lmin

mp3 OUTN C vdd 0 nfet w=10n l=lmin

mp4 OUT OUTN vdd 0 nfet w=10n l=lmin

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* pfet TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mn1 OUTN A AA vdd pfet w=10n l=lmin

mn2 AA B BB vdd pfet w=10n l=lmin

mn3 BB C 0 vdd pfet w=10n l=lmin

mn4 OUT OUTN 0 vdd pfet w=10n l=lmin

.ends

.subckt OR4in A B C D OUT

mp1 OUTN A vdd 0 nfet w=10n l=lmin

mp2 OUTN B vdd 0 nfet w=10n l=lmin

mp3 OUTN C vdd 0 nfet w=10n l=lmin

mp4 OUTN D vdd 0 nfet w=10n l=lmin

mp5 OUT OUTN vdd 0 nfet w=10n l=lmin

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* pfet TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mn1 OUTN A AA vdd pfet w=10n l=lmin

mn2 AA B BB vdd pfet w=10n l=lmin

mn3 BB C CC vdd pfet w=10n l=lmin

mn4 CC D 0 vdd pfet w=10n l=lmin

mn5 OUT OUTN 0 vdd pfet w=10n l=lmin

.ends

\*.subckt OR5in A B C D E OUT

\*mp1 OUTN A vdd vdd pfet w=10n l=lmin

\*mp2 OUTN B vdd vdd pfet w=10n l=lmin

\*mp3 OUTN C vdd vdd pfet w=10n l=lmin

\*mp4 OUTN D vdd vdd pfet w=10n l=lmin

\*mp5 OUTN E vdd vdd pfet w=10n l=lmin

\*mp6 OUT OUTN vdd vdd pfet w=10n l=lmin

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* nfet TRANSISTORS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*mn1 OUTN A AA 0 nfet w=10n l=lmin

\*mn2 AA B BB 0 nfet w=10n l=lmin

\*mn3 BB C CC 0 nfet w=10n l=lmin

\*mn4 CC D DD 0 nfet w=10n l=lmin

\*mn5 DD E 0 0 nfet w=10n l=lmin

\*mn6 OUT OUTN 0 0 nfet w=10n l=lmin

\*.ends

.subckt cla a0 a1 a2 a3 b0 b1 b2 b3 g0 g1 g2 g3 p0 p1 p2 p3

XXOR1 a0 b0 p0 XOR

XXOR2 a1 b1 p1 XOR

XXOR3 a2 b2 p2 XOR

XXOR4 a3 b3 p3 XOR

XAND2in1 a0 b0 g0 AND2in

XAND2in2 a1 b1 g1 AND2in

XAND2in3 a2 b2 g2 AND2in

XAND2in4 a3 b3 g3 AND2in

.ends

.subckt cgen c0 g0 g1 g2 g3 p0 p1 p2 p3 c1 c2 c3 G P

XAND2in5 c0 p0 y0 AND2in

XAND3in1 c0 p0 p1 y1 AND3in

XAND2in6 g0 p1 y2 AND2in

XAND4in1 c0 p0 p1 p2 y3 AND4in

XAND3in2 g0 p1 p2 y4 AND3in

XAND2in7 g1 p2 y5 AND2in

XAND4in2 p0 p1 p2 p3 P AND4in

XAND4in3 g0 p1 p2 p3 y7 AND4in

XAND3in3 g1 p2 p3 y8 AND3in

XAND2in8 g2 p3 y9 AND2in

XOR2in1 y0 g0 c1 OR2in

XOR3in1 y1 y2 g1 c2 OR3in

XOR4in1 y3 y4 y5 g2 c3 OR4in

XOR4in2 y7 y8 y9 g3 G OR4in

.ends

.subckt sum c0 c1 c2 c3 p0 p1 p2 p3 s0 s1 s2 s3

XXOR5 c0 p0 s0 XOR

XXOR6 c1 p1 s1 XOR

XXOR7 c2 p2 s2 XOR

XXOR8 c3 p3 s3 XOR

.ends

Xcla1 a0 a1 a2 a3 b0 b1 b2 b3 g0 g1 g2 g3 p0 p1 p2 p3 cla

Xcla2 a4 a5 a6 a7 b4 b5 b6 b7 g4 g5 g6 g7 p4 p5 p6 p7 cla

Xcla3 a8 a9 a10 a11 b8 b9 b10 b11 g8 g9 g10 g11 p8 p9 p10 p11 cla

Xcla4 a12 a13 a14 a15 b12 b13 b14 b15 g12 g13 g14 g15 p12 p13 p14 p15 cla

Xcgen1 c0 g0 g1 g2 g3 p0 p1 p2 p3 c1 c2 c3 ga1 pa1 cgen

Xcgen2 c0 g4 g5 g6 g7 p4 p5 p6 p7 c4 c5 c6 ga2 pa2 cgen

Xcgen3 c0 g8 g9 g10 g11 p8 p9 p10 p11 c7 c8 c9 ga3 pa3 cgen

Xcgen4 c0 g12 g13 g14 g15 p12 p13 p14 p15 c10 c11 c12 ga4 pa4 cgen

Xcgen5 c0 ga1 ga2 ga3 ga4 gp1 gp2 gp3 gp4 cx1 cx2 cx3 gx1 px1 cgen

Xsum1 c0 c1 c2 c3 p0 p1 p2 p3 s0 s1 s2 s3 sum

Xsum2 c4 c5 c6 c7 p4 p5 p6 p7 s4 s5 s6 s7 sum

Xsum3 c8 c9 c10 c11 p8 p9 p10 p11 s8 s9 s10 s11 sum

Xsum4 c12 c13 c14 c15 p12 p13 p14 p15 s12 s13 s14 s15 sum

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* MEASUREMENTS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

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.measure tran average\_power avg power from=0ns to=LenTran

.measure tran peak\_power max power from=0ns to=LenTran

.end